Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec– 2017**

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| **Code :** | **17EC3032** | **Duration :** | **3hrs** |
| **Sub. Name :** | **CMOS VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Calculate the threshold voltage VTO at VSB = 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density NA=1016 cm-3, polysilicon gate doping density ND=2x1020 cm-3, gate oxide thickness tox=500Å, and oxide interface fixed charge density Nox = 4x1010cm-2 . | CO1 | 10 |
| b. | Derive the expressions for threshold voltage Structure and Channel length Modulation of a MOS structure. | CO2 | 10 |
| (OR) | | | | |
| 2. | a. | Discuss about equivalent resistor using a small signal model MOS Structure. | CO2 | 10 |
| b. | Discuss in detail about the Oxide and Junction capacitances. | CO1 | 10 |
| 3. | a. | Design the basic Boolean functional unit using CMOS transistor logic.  Y = ((A.B.C)+D) and Y= (A +(B.C + D)) | CO5 | 12 |
|  | b. | With neat diagram explain in detail about PMOS design rule. | CO3 | 8 |
| (OR) | | | | |
| 4. |  | Explain the DC and transfer characteristics of CMOS inverter and derive the expression for output voltage in various operating regions. | CO4 | 20 |
| 5. | a. | Define ratioed logic and explain in detail about Dynamic Latches and Registers. | CO3 | 10 |
|  | b. | With neat diagram explain in detail about DCVSL and pass transistor logic. | CO3 | 10 |
| (OR) | | | | |
| 6. | a. | Design the basic Boolean functional unit using CMOS Switch logic. Y = ((A+B+C).D) with its stick diagram. | CO5 | 12 |
|  | b. | What are design rules? Explain all the types of rules with necessary schematic. | CO3 | 8 |
| 7. | a. | With neat timing diagram explain in detail about np-CMOS logic. | CO5 | 10 |
|  | b. | Explain about Pass transistor logic in static CMOS design. | CO3 | 10 |
| (OR) | | | | |
| 8. |  | With neat diagram explain in detail about clocked CMOS logic (C2MOS) and design 3-input NAND gate using clocked CMOS (C2MOS) logic. | CO5 | 20 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Explain in detail about Dynamic CMOS logic and design the following Boolean expression using Dynamic CMOS Logic.  Z = AB + (C + D)(E + F). | CO5 | 14 |
|  | b. | Explain the general rules to describe the color codes used in stick diagram also brief the step by step procedure to draw the Euler’s Path algorithm with suitable example. | CO3 | 6 |

ALL THE BEST